

In the Claims:

Please amend the claims as indicated below. This listing of claims replaces all prior versions.

1. (Currently amended) An integrated circuit comprising:

a logic path that is clocked by a clock signal; and

a timing closure monitoring circuit for monitoring timing closure in a the logic path, ~~on the integrated circuit, the logic path being clocked by a clock signal, and the~~ timing closure monitoring circuit ~~comprising~~ including:

a signal generator for generating a predetermined reference signal;

a duplicate logic path having timing characteristics matched with the logic path being monitored, and connected to receive the reference signal from the signal generator; and

a monitoring circuit arranged to receive an output signal from the duplicate logic path, to compare receipt of the output signal relative to receipt of the clock signal, and to provide a timing closure signal indicative of the status of the timing closure in the logic path being monitored responsive to comparing the receipt of the output signal relative to receipt of the clock signal.

2. (Currently amended) An integrated circuit as claimed in claim 1, wherein the timing closure signal indicates a timing closure violation when the output signal of the duplicate logic path is delayed by a predetermined amount, and further comprising:

a first pipeline stage that includes the logic path being monitored;

a second pipeline stage that includes another logic path that is clocked by the clock signal, the first and second pipeline stages being serially connected,

wherein the timing closure monitoring circuit is configured and arranged to monitor timing closure in the other logic path being monitored, and the timing closure monitoring circuit further includes:

another signal generator for generating another predetermined reference signal;

another duplicate logic path having timing characteristics matched with the other logic path being monitored, and connected to receive the other reference signal from the other signal generator; and

another monitoring circuit arranged to receive an output signal from the other duplicate logic path, to compare receipt of the output signal from the other duplicate logic path relative to receipt of the clock signal, and to provide another timing closure signal indicative of the status of the timing closure in the other logic path being monitored responsive to comparing the receipt of the output signal from the other duplicate logic path relative to receipt of the clock signal.

3. (Previously presented) An integrated circuit as claimed in claim 1, wherein the clock signal is used by the signal generator to generate the reference signal, and wherein the timing closure signal indicates a timing closure violation when the output signal of the duplicate logic path is received by the monitoring circuit after the monitoring circuit receives a next leading edge of the clock signal.
4. (Original) An integrated circuit as claimed in claim 3, wherein the reference signal produced by the signal generator is synchronized with the clock signal.
5. (Original) An integrated circuit as claimed in claim 4, wherein the reference signal is synchronized with the leading edge of the clock signal.
6. (Previously presented) An integrated circuit as claims in claim 3, wherein the reference signal produced by the signal generator is delayed with respect to the clock signal.
7. (Original) An integrated circuit as claimed in claim 6, wherein the reference signal is delayed with respect to the clock signal by an amount equal to $(\text{prop_delay}) - (\frac{1}{2} \text{ design_margin})$, where prop_delay is the propagation delay of a processing unit driving the logic path, and the design margin relates to the sensitivity of the circuit for detecting timing closure.

8. (Previously presented) An integrated circuit as claimed in claim 1, wherein the signal generator is configured to generate a reference signal having a pulse width that is predetermined according to a design margin.
9. (Original) An integrated circuit as claimed in claim 8, wherein the design margin determines the sensitivity of the timing closure monitoring circuit for detecting timing closure violation.
10. (Previously presented) An integrated circuit as claimed in claim 1, wherein the duplicate logic path is configured to match the delay and/or composition characteristics of the logic path being monitored.
11. (Original) An integrated circuit as claimed in claim 10, wherein the duplicate logic path includes one or more buffer stages for matching the characteristics of the logic path being monitored.
12. (Previously presented) An integrated circuit as claimed in claim 11, wherein the one or more buffer stages comprise the same number of switching gates as the logic path being monitored.
13. (Currently amended) An integrated circuit as claimed in claim 2, wherein at least one of the timing closure violation signals is used to generate an interrupt signal.
14. (Currently amended) An integrated circuit as claimed in claim 2, wherein the timing closure violation signal provided by the monitoring circuit is supplied to the other monitoring circuit ~~a second timing closure monitoring circuit on the integrated circuit~~, the ~~first and second timing closure~~ monitoring circuits are configured and arranged to generate ~~generating~~ a serial interrupt signal.
15. (Currently amended) An integrated circuit as claimed in claim 2 [[1]], wherein the first pipeline stage includes a plurality of logic paths and the logic path being monitored is a critical path of the first pipeline stage, and the second pipeline stage includes a

plurality of logic paths and the other logic path being monitored is a critical path of the second pipeline stage in the integrated circuit.

16. (Previously presented) An integrated circuit as claimed in claim 1, having one or more further timing closure monitoring circuits, for monitoring timing closure in one or more further logic paths on the integrated circuit.

17. (Previously presented) An integrated circuit as claimed in claim 1, wherein the monitoring circuit includes a latch.

18. (Previously presented) An integrated circuit as claimed in claim 1, wherein the timing closure signal is used to control the timing closure in the logic path being monitored.

19. (Currently amended) A method of monitoring timing closure in a logic path on an integrated circuit, the logic path being clocked by a clock signal, the method comprising:

generating a predetermined reference signal;

providing a duplicate logic path corresponding to the logic path being monitored;
~~the logic path being clocked by a clock signal;~~

passing the reference signal through the duplicate logic path, and

monitoring receipt of the output of the duplicate logic path relative to receipt of the clock signal, and using the output of the duplicate logic path to produce a timing closure signal indicative of the status of the timing closure in the logic path being monitored based on the monitoring of the receipt of the output of the duplicate logic path relative to the receipt of the clock signal.

20. (Currently amended) A method as claimed in claim 19, wherein the timing closure signal indicates a timing closure violation when the output of the duplicate logic path is delayed by a predetermined amount, and wherein the integrated circuit includes a first pipeline stage that includes the logic path being monitored and a second pipeline stage that includes another logic path that is clocked by the clock signal, the pipeline stages being serially connected, the method further comprising monitoring timing closure in the other logic path by

generating another predetermined reference signal;
providing another duplicate logic path corresponding to the other logic path being monitored;
passing the other reference signal through the other duplicate logic path, and
monitoring receipt of the output of the other duplicate logic path relative to receipt of the clock signal, and using the output of the other duplicate logic path to produce another timing closure signal indicative of the status of the timing closure in the other logic path being monitored based on the monitoring of the receipt of the output of the other duplicate logic path relative to the receipt of the clock signal.

21. (Previously presented) A method as claimed in claim 19, wherein the clock signal is used to generate the reference signal, and wherein the timing closure signal indicates a timing closure violation when a next leading edge of the clock signal precedes the output of the duplicate logic path.

22. (Original) A method as claimed in claim 21, wherein the reference signal is synchronized with the clock signal.

23. (Original) A method as claimed in claim 22, wherein the reference signal is delayed with respect to the clock signal.

24. (Original) A method as claimed in claim 23, wherein the reference signal is delayed with respect to the clock signal by an amount equal to $(\text{prop_delay}) - (\frac{1}{2} \text{ design_margin})$, where prop_delay is the propagation delay of a processing unit driving the logic path, and the design margin relates to the sensitivity of the circuit for detecting timing closure.

25. (Previously presented) A method as claimed in claim 19, wherein the pulse width of the reference signal is chosen according to a predetermined design margin.

26. (Original) A method as claimed in claim 25, wherein the design margin relates to the sensitivity of the timing closure monitoring circuit for detecting timing closure violation.

27. (Previously presented) A method as claimed in claim 19, wherein the duplicate logic path is configured to match the delay and/or composition characteristics of the logic path being monitored.

28. (Previously presented) A method as claimed in any claim 19, wherein the logic path being monitored is a critical path in the integrated circuit.

29. (Currently amended) A method as claimed in claim 19, wherein the logic path being monitored is part of a pipeline stage that includes a plurality of logic paths and the logic path being monitored is a critical path of the pipeline stage, and wherein the step of providing the duplicate logic path is initially determined by includes:

- identifying ~~[[a]]~~ the critical logic path in the pipeline stage ~~integrated circuit~~;
- decomposing the critical path into one or more stages;
- constructing buffer stages corresponding to the stages identified in the decomposing step, the buffer stages being constructed to have the same characteristics as the stages of the critical path ~~being monitored~~; and
- composing the duplicate path using the buffer stages constructed in the constructing step.